(c) Built in EPROM programmer allowing files/programs to be archived using external plug in EPROM packs as the storage medium.

(d) RS232 port for printer connections or the interchange of files with another Z88, a BBC Micro or an IBM compatible.

(e) State of the art 'supertwist' liquid crystal display, with 8 lines x 106 characters format.

2. BUILD STANDARD

2.1 There are two build standards of the Z88 Computer in UK circulation, an early model using Issue 3 pcb artwork and the current model (November 1987) using Issue 4 artwork. Although electrically identical to the Issue 4 pcb Issue 3 is recognisable by the small number of hand soldered components added as a result of early development work. On the Issue 4 pcb the components have been incorporated as part of the revised artwork.

2.2 A further version of the Z88 is envisaged for the American market. This will have a metallised case interior and additional pcb components designed to reduce RFI emission to the statutory level.

3. ARCHITECTURE

3.1 The architecture of the Z88 computer, shown in Figure 1.4, is characterised by the small chip count. They include a CMOS version of the Z80 microprocessor, a 128k byte EPROM and a 32k byte RAM. A customised gate array connected between the CPU and the memory completes the basic design, providing the memory, liquid crystal display (LCD) and RS232 interfaces. The keyboard interface with the CPU is via the computer data and address buses.

3.2 Figure 1.5 shows the LCD and RS232 interfaces together with the discrete power circuit. The latter includes the power supply, fed either from the internal batteries or a plug in mains adaptor, and various monitoring circuits designed to sense abnormal circuit conditions and effect an ordered shut down of the machine. The gate array 'sense' line used for this purpose also monitors the memory and peripheral expansion slots, shutting the machine down whever a memory or peripheral card is inserted or removed.

3.3 Machine States

3.3.1 For diagnostic purposes, it is important to recognize that the Z88 has four operational states. These are:

(a) Active : Z80 clock running and the LCD display on (ie Z80 running program instructions).

(b) Snooze : Z80 clock stopped and the LCD display on (ie Z80 waiting for a keyboard input).

(c) Doze : Z80 clock running and the LCD display off (ie programming the plug-in EPROM).

(d) Coma : Z80 clock stopped and LCD display off (ie Z88 shut down).

4. Z80 CPU

4.1 The CPU is CMOS version of the Z80 microprocessor, chosen for its low working and standby power consumption. The standby power mode is selected by the CPU whenever possible (eg when it is waiting for a keyboard input) by executing the HALT instruction. The HALT output, sensed by the gate array results in the latter stopping the 3.2768 MHz CPU clock, in turn inducing the standby power mode. Normal CPU working is resumed when the clock is restored and the gate array requests an interrupt.

4.2 The CPU has a standard three bus input/output arrangement comprising the data bus, address bus and control bus.

4.3 **Data Bus.** D7 - D0 constitutes an 8-bit bi-directional data bus with active high, tri-state input/outputs. It is used during keyboard scanning, for exchanges with the gate array (in particular with the memory over the memory data bus MDH-MDA) and is available on the peripheral expansion connector PL8.

4.4 **Address Bus.** A15 - A0 constitutes a 16-bit address bus with active high tri-state outputs. It is used to set up addresses for the gate array (in particular with the memory on memory address bus MA19 - MA0), for keyboard scanning (A15 - A8 only) and is available on the peripheral expansion connectors PL8 and PL9.

4.5 **Control Bus.** The control bus is a collection of individual signals which generally organise the flow of data between the CPU and the gate array on the address and data buses. All signals are available on the peripheral expansion connectors and are described below:

(a) Maskable Interrupt ($\overline{INT}$) - active low signal generated by the gate array to call the CPU's maskable interrupt routine. As part of this routine the CPU reads the interrupt register in the gate array to determine the cause of the interrupt and therefore what action to take. Two machine states trigger this interrupt, battery low, signalled by the power supply, and the keyboard scan request. Battery low simply causes the LCD to display the BAT LOW legend, the keyboard scan request causes the CPU to scan the keyboard lines to detect whether any keys are pressed.