(b) Non-Maskable Interrupt ($\overline{NMI}$) - active low signal generated by the gate array to call the CPU's non-maskable interrupt routine. This routine is responsible for saving the current status of the machine prior to executing the HALT instruction. On receipt of the resultant HALT signal from the CPU the gate array induces the coma state. An NMI is generated by the gate array when the time-out set up using the panel options expires, the memory slot flap is opened or in response to the external sense signal SNS. The latter is generated in the event of a power supply failure or if a plug in memory/peripheral card is inserted/removed.

(c) $\overline{HALT}$ is an active low signal generated when the CPU executes a HALT instruction. HALT can be generated autonomously by the CPU to induce the snooze state or in response to the NMI interrupt to induce the coma state.

(d) Memory Request ($\overline{MREQ}$) - this signal is active low indicating when the address bus holds a valid address for a memory read/write operation.

(e) Input/Output Request ($\overline{IORQ}$) - this signal is active low when the address bus holds a valid address for a gate array register read/write operation or when the CPU is scanning the keyboard.

(f) Machine Cycle 1 ($\overline{M1}$) - this signal is active low when the CPU is executing the first cycle of a multi-machine cycle instruction. Using M1 the gate array can determine when the CPU is writing to memory or conducting a refresh cycle (see para. 6.6.3). The use of this signal saves a pin on the gate array which would otherwise have to receive both the CPU write ($\overline{WR}$) and refresh ($\overline{RFSH}$) signals.

(g) The read/write signals ($\overline{RD}$ and $\overline{WR}$) are active low, one or other being asserted when the CPU wants to read or write data to a memory location, or a register in the gate array. Both signals are available on the peripheral interface connector SK9; only $\overline{RD}$ is supplied to the gate array.

(h) Reset ($\overline{RST}$) - active low signal output from the gate array when the reset pushbutton SW1 is pressed. The effect of operating the reset pushbutton is discussed below.

4.6 **Reset Operation.** Two operations of the pushbutton are required to effect a reset, one to start the CPU clock (since for a large proportion of the time the CPU will be in the snooze state) and the second which the CPU can then act upon. The reset pulses themselves (RIN on IC4 pin 97 and $\overline{RST}$ on IC1 pin 26) reset the circuits within the gate array and cause the CPU to effect a restart. The latter results in the CPU clearing certain internal registers and then running the restart routine. The outcome of this routine is dependent on the state of the flap input to the gate array on IC4 pin 92 which the CPU reads during an I/O read cycle. If the memory card slot flap is open (FLP high) the routine effects a hard reset clearing the RAM memory. Alternatively, if the flap is closed (FLP low) a soft reset occurs erasing only the suspended activities (see the Z88 User Guide for further details).