5. SYSTEM CLOCKS

5.1 The Z88 has two system clocks - a low power 25.6 KHz clock active during the machine's coma state, and a 9.8304 MHz master clock active at all other times.

5.2 Referring to Figure 1.6, crystal oscillator TR18/XT1 generates the master clock, the resultant signal MCK being divided in the gate array to produce a 3.278 MHz clock for the CPU on IC1 pin 6 and the LCD on SK5 pin 9. Typically, the clock consumes 2 mA and is switched off to conserve battery life by suppressing the +5.5V switched power rail (see para. 10.3.1).

5.3 Crystal XT2 sources the standby clock SCK, buffered by TR19/24. This signal is always presented to the gate array but is only effective when the machine is in coma. In the coma state, SCK maintains the real-time clock and drives the minimum amount of circuitry required to monitor the keyboard inputs.

6. MEMORY ORGANISATION

6.1 Internal memory for the Z88 is provided by a 32k byte pseudo-static RAM and a 128k byte EPROM. External RAM in the form of plug-in memory cards increases the available RAM by up to 3m bytes. Three slots each accept a 32k byte or 128k byte memory card with a 1m byte memory card promised for early 1988.

6.2 Slot 3 has a dual function, accepting either a RAM or EPROM memory card. The latter (also available in three standard sizes) is used to archive files using the Z88's built-in EPROM programmer. (ROM memory cards are also available for test purposes and can be plugged into any of the slots).

6.3 Suffice it to say, it is necessary for the CPU to know the size and type of memory card in each of the slots. This information is determined when the CPU conducts selective read/write cycles to memory during power up and, in the case of slot 3, when the EPROM options are selected from the Filer menu.

6.4 Memory Addressing

6.4.1 The maximum addressable memory is 4m bytes, divided between 1m byte of internal memory (½m byte each for RAM and EPROM) and 1m byte for each memory card slot.

6.4.2 Since the CPU's address bus limits direct memory access to 64k bytes, the width of the bus must be increased from 16 to 21 bits. This function is carried out using four address extension registers in the gate array located in the CPU's I/O address space (see Figure 1.1).