6.5 Read/Write Operations (Figure 1.6)

6.5.1 Memory read/write operations are decoded by the gate array using the $\overline{M1}$, $\overline{RD}$ and $\overline{MREQ}$ inputs from the CPU, and address bits A21 - A19 held in the address extension registers.

6.5.2 **Internal EPROM (IC3).** Read cycles for IC3 are preceded by writing all 0's to bits A21 - A19 of the appropriate address extension register within IC4. When the CPU enables the register, these bits are decoded to produce the active low chip enable signal for the EPROM, output as IPCE on IC4 pin 68.

The active low output enable signal for IC3 is also decoded within IC4 from the $\overline{M1}$, $\overline{RD}$ and $\overline{MREQ}$ waveforms generated by the CPU during an instruction opcode fetch. In the appropriate combination, these signals generate ROE on IC4 pin 87, causing the EPROM to output data to IC4 on MDH - MDA from an address specified by MA15 - MA0. The latter comprises bits A13 - A0 output by the CPU as CA0 - CA13, and the bottom two bits of the gate array's address extension register. Data received from EPROM is gated within IC4 and presented to the CPU as CDH - CDA.

6.5.3 **Internal RAM (IC2).** Read/write cycles for IC2 are preceded by writing 0's into bits A21 and A20 of the appropriate address extension register and a 1 into A19. When the CPU enables the register, these bits are decoded to produce the active low chip enable signal for the RAM, output as IRCE on IC4 pin 39. The active low output enable signal for IC2 is also decoded within IC4, as in the case of the EPROM, to produce POE on IC4 pin 87. Likewise, a memory read or memory write cycle is determined by IC4 from the state of M1, MREQ and $\overline{RD}$ waveforms. IC4 pin 63 ($\overline{WR}$) is high for a read cycle and low for a write cycle.

NOTE: The printed circuit board is tracked for a 32-pin 128k byte RAM device. The circuit diagram is similarly configured. For the current 32k RAM device, pin 3 is read as pin 1, A16, A15 and POE are not used, and the $\overline{CS}$ signal (pin 28 on the 32k RAM) is VCC. In all other respects, the pinout of the two devices is identical.

6.5.4 **External RAM.** External RAM in slots 1 to 3 is accessed in a similar manner to the internal RAM except for the chip enable signals. Instead of IRCE, the gate array decodes the top two bits of the address extension register to produce individual slot enable signals SE1 to SE3 on IC4 pins 86, 93 and 91 respectively.

6.5.5 The top three bits of the address bus MA16 to MA19 are also available to each slot allowing up to 1m byte of memory to be addressed.