6.5.6 External EPROM.

TBD - Awaiting input from Cambridge Computer

6.6 Memory Refresh

6.6.1 The internal and external RAM is known as pseudo-static RAM, combining the high density/low cost benefits of a dynamic RAM with the static RAM's ability to retain data without the need for external refresh circuitry. Instead, refresh is carried out using the memory's on-chip refresh circuitry or, as is the normal case, when addressing the RAM to update the LCD display frame.

6.6.2 On-chip refresh, enabled only when the Z88 is in the coma state or the CPU is programming an EPROM, is achieved by simultaneously holding the $\overline{CE}$ line to each RAM high (ie IRCE, and SE1 to SE3), and the $\overline{OE}$/$\overline{RFSH}$ line low (ie POE). At all other times, the RAM address range produced whilst updating the LCD display frame is sufficient to keep the RAM contents refreshed.

6.6.3 The occurrence of a refresh cycle conducted by the CPU at the end of each opcode fetch instruction is sensed by the gate array from a decode of the $\overline{M1}$, $\overline{MREQ}$ and $\overline{RD}$ signals and the corresponding refresh address placed on the address bus ignored.

6.7 Bus Protection

6.7.1 As a precaution, the Z88 is forced into the coma state whenever a memory card (or peripheral card) is plugged into or removed from one of the external slots. Insertion or removal of a card is detected when the edge connector sense line is pulled down to 0V. When this occurs, the gate array generates a non-maskable interrupt to the CPU causing the latter to initiate a controlled shutdown (see also para. 11.3.3).

6.7.2 Shaping the lands on the memory card edge connectors in the region of pins 15 to 17 ensures that pin 15 (SNS) is shorted to pins 16 and 17 (0V), except when the card is fully inserted in the slot. Other edge connector lands are cut such that the sense line is grounded first before the address and data line connections are made or broken during card insertion/removal.

6.7.3 A similar scheme is adopted for the peripheral expansion card, except that the edge connector lands on the Z88 pcb are cut. In this case, two sense lines are provided in positions 1A and 24A so that the above criteria are satisfied even when the peripheral card is skewed.

7. EPROM PROGRAMMER

TBD - Awaiting input from Cambridge Computer