9.2   Scanning Routine

9.2.1   The scanning method is described below with the aid of Figure 1.3. As the figure clearly illustrates, the keyboard consists of an 8 x 8 matrix, the interconnection of each row and column bridged by a normally open switch contact. The row inputs and column outputs are shown connected to separate ribbon cables SK6 and SK7, the column inputs to the CPU's high order address lines CA15 - CA8 and the row outputs to the gate array and CPU on the data bus CDH to CDA (D7 - D0).

9.2.2   When the keyboard scanning routines are entered, the CPU performs successive I/O read cycles setting the $\overline{IOREQ}$ and $\overline{RD}$ lines to the gate array low. At the same time the I/O port addresses placed on the upper half of the address bus are modified with each cycle such that address lines A15 through A8 are set low in turn, the others remaining high. (NOTE: This set of addresses is not within the I/O address range of the gate array, thus the latter will not respond to the I/O read request).

9.2.3   The sequence starts with I/O address $8F_H$ driving address line A15 low. The keyboard matrix also sees this potential on column 1 applied via D14 and the ribbon cable SK6. Thus when any of the switches on the inter-section with column 1 is pressed, the corresponding row output supplying the CPU via the second ribbon cable (SK7), is pulled low. The row outputs drive the CPU data bus and are all pulled high by RP1 when none of the keys are pressed. For example, if the 'ESC' key is pressed, row 2 drives data bus D5 (CDE) low and so on.

The sequence ends with I/O address FE_H when column 7 is addressed. In this case, operation of the '5' key drives D5 low. Clearly, the keyboard scanning routines make the distinction between the 'ESC' and '5' keys by knowing which address line is being driven.

9.2.5   Between interrupts while the machine is waiting for a keyboard input, the CPU executes a HALT instruction causing the gate array to stop the CPU clock (snooze state). In this state, address lines A15 - A8 are all low. As a result, operation of any key will cause the respective data line to be pulled low. An AND gate in the gate array, monitoring the data bus, registers the key operation and after enabling the master clock to the CPU, generates a maskable interrupt immediately requesting a keyboard scan.

9.3   Turn on Sequence

9.3.1   In the coma state, when the CPU clock is stopped, the CPU must recognise operation of both SHIFT keys in order to turn the machine on. This is achieved as described in the previous paragraph except that when in coma the CPU only holds address lines A15 and A14 low. At the same time the gate array only monitors the state of data bits D7 and D6. When both data bits are low, any two of the following keys might be pressed - right-hand SHIFT, '|‾|', 'HELP' or left-hand SHIFT. To find out which, the gate arrays enables the clock to the CPU and drives the maskable interrupt line requesting an immediate keyboard scan. On detecting both SHIFT keys operated, the CPU writes to a register in the gate array prompting the latter to turn on the Z88.