(d) Check the following signals to find out if the pseudo-static RAM is being refreshed:

Signal	Level	Test Point
IRCE	High	IC2, pin 22
SE1	High	SK1, pin 30
SE2	High	SK2, pin 30
SE3	High	SK3, pin 30
POE	Low	IC2, pin 1

(e) If the signals in (d) above are not present, a serious fault exists. Check for 5.5V at R74 and trouble-shoot for a power supply fault if not present.

(f) Check for the 25.6 KHz clock at the collector of T24. If this signal is not present, the computer does not come out of the coma state.

(g) Check at C21 if the 40 µS reset pulses are reaching the gate array. The level is normally high and goes low for the duration of the pulse. Allow 1 second between pressings of the Reset switch.

CAUTION: DO NOT ATTEMPT TO MEASURE THE 9 MHz CLOCK WITH AN UNPROTECTED PROBE. USE A 1 nf CAPACITOR IN SERIES WITH THE PROBE OR ATTEMPT TO 'PICK UP' THE OSCILLATOR SIGNAL WITH THE PROBE CLOSE TO BUT NOT TOUCHING THE CIRCUIT.

(h) If the reset is present, use the frequency meter to check at R43 for the 9.83040 MHz clock signal. If the clock is not present, check at R42 for the switched 5.5V rail. If 5.5V is not present, check at R39 for a low LP signal from the gate array.

(j) Check at IC1 pin 26 that reset pulses from the gate array are getting through to the Z80. If reset pulses are present, check at IC1 pin 6 that 5.5V 3.2768 MHz pulses are present.

(k) If the Z80 is not being reset, check at the collector of R25 for a high level (+5.5V). If this is not present, the computer cannot leave the coma state.

(l) If no progress is being made check for correct operation of the Flap switch - normally open.