10. RS232C INTERFACE

10.1 The RS232C port is controlled by registers within the gate array accessed by the CPU during I/O read/write cycles to locations with address bit 4 (A3) set to 0. Single bit latches register the state of the interface control signals RTS, CTS and DCD; shift registers clocked at the selected baud rate perform the serial/parallel conversions for data transmission and reception. The physical port is presented on SK10, the conversion from RS232C levels to/from logic levels being carried out by discrete components (see Figure 1.6).

10.2 Output Circuits

10.2.1 Output circuits TXD and RTS, on the emitter of TR14 and TR15 respectively, switch between ±5V driven by outputs from the gate array on IC4 pins 37 and 38. When the gate array outputs are at +5V (logic 1) TR14 and TR15 are turned on, switching the respective output circuit to -6V. Conversely, when the array's outputs are at OV (logic 0) TR11 and TR12 are turned on, switching the respective output circuits to +5V.

10.3 Switched Power Rails

10.3.1 It will be noted that the -6V rail for the output circuits is switched via TR16, the latter controlled by TR13/17 and the line pulse output on IC4 pin 45. Except during the coma and doze states, when the display is turned off, LP filtered by R39/C10 turns TR17, TR13 and TR16 on, enabling both the +5.5V and -6V switched power rails. In the coma and doze states, LP and the base of TR17 are both held at +5.5V turning off all three transistors and the switched power rails. In this state, with IC4 pins 37 and 38 held at +5.5V, the TXD and RTS output circuits on SK10 are allowed to float.

10.4 Input Circuits

- 10.4.1 Input circuits RXD, CTS and DCD are routed to IC4 pins 41, 42 and 43 via identical resistor/diode networks. Zener diodes D9 D10 limit the excursion of the input signals to between +5.1V (logic 0) and -0.5V (logic 1); resistors R23, 26 and 29 maintain the inputs at OV when the interface is disconnected.
- 10.4.2 Resistor R82 attached between the body of SK10 and the +5.5V supply available on pin 1, serves as a discharge path for any static build-up on the mating connector.