11.3.4 A similar chain of events is triggered if the batteries are removed for replacement while the Z88 is turned on and in the snooze state. However, because in this state the clock to the CPU is stopped, the CPU will not immediately recognize the interrupt. Ordinarily this does not cause a problem, since within 10 mS of generating the interrupt the gate array restores the clock preparatory to requesting a keyboard scan. The CPU would then recognise the interrupt and take the necessary steps to shut down the machine. However, due to the limited capacity of the +5.5V storage capacitors C4/C5 and the need to conserve the charge on the supercapacitor C22 for the RAM during the battery change, shut-down must occur within approximately 1 mS of the interrupt occurring. This is effected by using the $\overline{\text{NMI}}$ to force an immediate keyboard interrupt by driving data bus D2 low via D30. The principle is described in para 9.2.5.

11.4 Power Supply and Voltage Regulator

11.4.1 The flyback converter comprises inductor L2 driven by the blocking oscillator TR5, C10 and R8. Energy stored in L2 while TR5 is turned on is released during flyback, charging the various storage capacitors via rectifiers D1 to D6.

With reference to the supply outputs, L1 and decoupling capacitors C5 and C24 to C27 together provide a smooth +5.5V supply, distributed within the Z88 as Vcc. +5.5V is chosen so as to meet the programming requirements of the plug-in EPROMs. D6 between the +5.5V and +12V rails limits the positive excursion of the +12V rail (which can rise to approximately ??V in the coma state) to +16.5V.

11.4.2 Supply regulation is provided by TR1 to TR4 which source drive for the blocking oscillator TR5. Z1 in the emitter circuit of TR1 senses the level of the +5.5V rail, turning TR1 off when the supply drops below +5.5V. TR1 off turns TR2/TR4 on sourcing drive current for TR5. As a result, TR5 is allowed to oscillate, restoring the level of the +5.5V rail. At this point, TR1 is turned on, TR1/TR4 turn off and oscillation of TR5 ceases. Feedback between TR4 emitter and TR1 base via R3 limits the gain of the regulator, preventing it from breaking into violent oscillation. R5 senses the drive current taken by TR5 turning on TR3 when the current drawn from battery exceeds ?? mA. In these circumstances, TR3 diverts drive current to TR5, shutting down the oscillator and with it the power supply.

11.4.3 TR9 monitors the current drawn from the +5.5V power rails, turning on when the emitter voltage goes sufficiently negative to forward bias the base emitter junction. This is only true when the -6V switched supply is enabled (ie the machine is not in the coma or doze state - see para. 10.3.1) and the voltage on TR1 emitter, as a result of excess current drawn from the +5.5V rail, drops to approximately 0V. Under these conditions, the voltage drop across D26 fixes TR9 emitter at approximately -0.5V and since the base is tied to 0V, TR9 turns on. TR9 turning on drives the sense line input to the gate array on IC4 pin 94, forcing the Z88 into the coma state as described in para. 11.3.3.