SECTION 1

SYSTEM DESCRIPTION

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1. INTRODUCTION

1.1 The Z88 Computer is a portable laptop machine incorporating many inovative features, not least of which is the computer's ability to selectively shut down large areas of the circuitry when not required, thus prolonging battery life. This expedient is designed to provide up to 20 hours of active computing time or up to one year in the standby mode during which time the contents of the resident memory are preserved.

1.2 Other important features include:

(a) 32k byte of internal RAM expandable by up to 3m byte using plug-in RAM packs.

(b) 128k byte of internal EPROM containing the operating system, BBC Basic interpreter and a powerful suite of applications software.

(c) Built in EPROM programmer allowing files/programs to be archived using external plug in EPROM packs as the storage medium.

(d) RS232 port for printer connections or the interchange of files with another Z88, a BBC Micro or an IBM compatible.

(e) State of the art 'supertwist' liquid crystal display, with 8 lines x 106 characters format.

2. BUILD STANDARD

2.1 There are two build standards of the Z88 Computer in UK circulation, an early model using Issue 3 pcb artwork and the current model (November 1987) using Issue 4 artwork. Although electrically identical to the Issue 4 pcb Issue 3 is recognisable by the small number of hand soldered components added as a result of early development work. On the Issue 4 pcb the components have been incorporated as part of the revised artwork.

2.2 A further version of the Z88 is envisaged for the American market. This will have a metallised case interior and additional pcb components designed to reduce RFI emission to the statutory level.

3. ARCHITECTURE

3.1 The architecture of the Z88 computer, shown in Figure 1.4, is characterised by the small chip count. They include a CMOS version of the Z80 microprocessor, a 128k byte EPROM and a 32k byte RAM. A customised gate array connected between the CPU and the memory completes the basic design, providing the memory, liquid crystal display (LCD) and RS232 interfaces. The keyboard interface with the CPU is via the computer data and address buses.

3.2 Figure 1.5 shows the LCD and RS232 interfaces together with the discrete power circuit. The latter includes the power supply, fed either from the internal batteries or a plug in mains adaptor, and various monitoring circuits designed to sense abnormal circuit conditions and effect an ordered shut down of the machine. The gate array 'sense' line used for this purpose also monitors the memory and peripheral expansion slots, shutting the machine down whever a memory or peripheral card is inserted or removed.

3.3 Machine States

3.3.1 For diagnostic purposes, it is important to recognize that the Z88 has four operational states. These are:

(a) Active : Z80 clock running and the LCD display on (ie Z80 running program instructions).

(b) Snooze : Z80 clock stopped and the LCD display on (ie Z80 waiting for a keyboard input).

(c) Doze : Z80 clock running and the LCD display off (ie programming the plug-in EPROM).

(d) Coma : Z80 clock stopped and LCD display off (ie Z88 shut down).

4. Z80 CPU

4.1 The CPU is CMOS version of the Z80 microprocessor, chosen for its low working and standby power consumption. The standby power mode is selected by the CPU whenever possible (eg when it is waiting for a keyboard input) by executing the HALT instruction. The HALT output, sensed by the gate array results in the latter stopping the 3.2768 MHz CPU clock, in turn inducing the standby power mode. Normal CPU working is resumed when the clock is restored and the gate array requests an interrupt.

4.2 The CPU has a standard three bus input/output arrangement comprising the data bus, address bus and control bus.

4.3 **Data Bus.** D7 - D0 constitutes an 8-bit bi-directional data bus with active high, tri-state input/outputs. It is used during keyboard scanning, for exchanges with the gate array (in particular with the memory over the memory data bus MDH-MDA) and is available on the peripheral expansion connector PL8.

4.4 **Address Bus.** A15 - A0 constitutes a 16-bit address bus with active high tri-state outputs. It is used to set up addresses for the gate array (in particular with the memory on memory address bus MA19 - MA0), for keyboard scanning (A15 - A8 only) and is available on the peripheral expansion connectors PL8 and PL9.

4.5 **Control Bus.** The control bus is a collection of individual signals which generally organise the flow of data between the CPU and the gate array on the address and data buses. All signals are available on the peripheral expansion connectors and are described below:

(a) Maskable Interrupt ($\overline{INT}$) - active low signal generated by the gate array to call the CPU's maskable interrupt routine. As part of this routine the CPU reads the interrupt register in the gate array to determine the cause of the interrupt and therefore what action to take. Two machine states trigger this interrupt, battery low, signalled by the power supply, and the keyboard scan request. Battery low simply causes the LCD to display the BAT LOW legend, the keyboard scan request causes the CPU to scan the keyboard lines to detect whether any keys are pressed.

(b) Non-Maskable Interrupt ($\overline{NMI}$) - active low signal generated by the gate array to call the CPU's non-maskable interrupt routine. This routine is responsible for saving the current status of the machine prior to executing the HALT instruction. On receipt of the resultant HALT signal from the CPU the gate array induces the coma state. An NMI is generated by the gate array when the time-out set up using the panel options expires, the memory slot flap is opened or in response to the external sense signal SNS. The latter is generated in the event of a power supply failure or if a plug in memory/peripheral card is inserted/removed.

(c) $\overline{HALT}$ is an active low signal generated when the CPU executes a HALT instruction. HALT can be generated autonomously by the CPU to induce the snooze state or in response to the NMI interrupt to induce the coma state.

(d) Memory Request ($\overline{MREQ}$) - this signal is active low indicating when the address bus holds a valid address for a memory read/write operation.

(e) Input/Output Request ($\overline{IORQ}$) - this signal is active low when the address bus holds a valid address for a gate array register read/write operation or when the CPU is scanning the keyboard.

(f) Machine Cycle 1 ($\overline{M1}$) - this signal is active low when the CPU is executing the first cycle of a multi-machine cycle instruction. Using M1 the gate array can determine when the CPU is writing to memory or conducting a refresh cycle (see para. 6.6.3). The use of this signal saves a pin on the gate array which would otherwise have to receive both the CPU write ($\overline{WR}$) and refresh ($\overline{RFSH}$) signals.

(g) The read/write signals ($\overline{RD}$ and $\overline{WR}$) are active low, one or other being asserted when the CPU wants to read or write data to a memory location, or a register in the gate array. Both signals are available on the peripheral interface connector SK9; only $\overline{RD}$ is supplied to the gate array.

(h) Reset ($\overline{RST}$) - active low signal output from the gate array when the reset pushbutton SW1 is pressed. The effect of operating the reset pushbutton is discussed below.

4.6 **Reset Operation.** Two operations of the pushbutton are required to effect a reset, one to start the CPU clock (since for a large proportion of the time the CPU will be in the snooze state) and the second which the CPU can then act upon. The reset pulses themselves (RIN on IC4 pin 97 and $\overline{RST}$ on IC1 pin 26) reset the circuits within the gate array and cause the CPU to effect a restart. The latter results in the CPU clearing certain internal registers and then running the restart routine. The outcome of this routine is dependent on the state of the flap input to the gate array on IC4 pin 92 which the CPU reads during an I/O read cycle. If the memory card slot flap is open (FLP high) the routine effects a hard reset clearing the RAM memory. Alternatively, if the flap is closed (FLP low) a soft reset occurs erasing only the suspended activities (see the Z88 User Guide for further details).

5. SYSTEM CLOCKS

5.1 The Z88 has two system clocks - a low power 25.6 KHz clock active during the machine's coma state, and a 9.8304 MHz master clock active at all other times.

5.2 Referring to Figure 1.6, crystal oscillator TR18/XT1 generates the master clock, the resultant signal MCK being divided in the gate array to produce a 3.278 MHz clock for the CPU on IC1 pin 6 and the LCD on SK5 pin 9. Typically, the clock consumes 2 mA and is switched off to conserve battery life by suppressing the +5.5V switched power rail (see para. 10.3.1).

5.3 Crystal XT2 sources the standby clock SCK, buffered by TR19/24. This signal is always presented to the gate array but is only effective when the machine is in coma. In the coma state, SCK maintains the real-time clock and drives the minimum amount of circuitry required to monitor the keyboard inputs.

6. MEMORY ORGANISATION

6.1 Internal memory for the Z88 is provided by a 32k byte pseudo-static RAM and a 128k byte EPROM. External RAM in the form of plug-in memory cards increases the available RAM by up to 3m bytes. Three slots each accept a 32k byte or 128k byte memory card with a 1m byte memory card promised for early 1988.

6.2 Slot 3 has a dual function, accepting either a RAM or EPROM memory card. The latter (also available in three standard sizes) is used to archive files using the Z88's built-in EPROM programmer. (ROM memory cards are also available for test purposes and can be plugged into any of the slots).

6.3 Suffice it to say, it is necessary for the CPU to know the size and type of memory card in each of the slots. This information is determined when the CPU conducts selective read/write cycles to memory during power up and, in the case of slot 3, when the EPROM options are selected from the Filer menu.

6.4 Memory Addressing

6.4.1 The maximum addressable memory is 4m bytes, divided between 1m byte of internal memory (½m byte each for RAM and EPROM) and 1m byte for each memory card slot.

6.4.2 Since the CPU's address bus limits direct memory access to 64k bytes, the width of the bus must be increased from 16 to 21 bits. This function is carried out using four address extension registers in the gate array located in the CPU's I/O address space (see Figure 1.1).

6.4.3 The bottom six bits of each 8-bit register (A19 - A14) provide a page address in the range 0 - 63, each page comprising 16k locations. This page reference, combined with the page offset address provided by the CPU on A13 - A0 allows access to any address in the range 0 - 1 Mbyte. Which 1m byte segment of the 4m byte memory space is addressed in this way is determined by the top two bits in each extension register (A21 and A20). Internal memory occupies segment 0 and slots 1 to 3, segments 1, 2 and 3 respectively.

6.4.4 The extension register chosen to supply the page and segment address is determined by A15 and A14 output on the CPU address bus together with the page offset. This feature is useful since it allows the CPU to set up the registers once prior to accessing any contiguous 64k byte block of memory.

6.4.5 Access to either the EPROM or RAM resident within segment 0 is determined by address A19 within the appropriate extension register. A19 set high selects EPROM in the lower ½m byte, and when set low selects RAM in the upper ½m byte.

6.4.6 CPU access to the extension registers is using an I/O write instruction which also requires address bit A3 high.

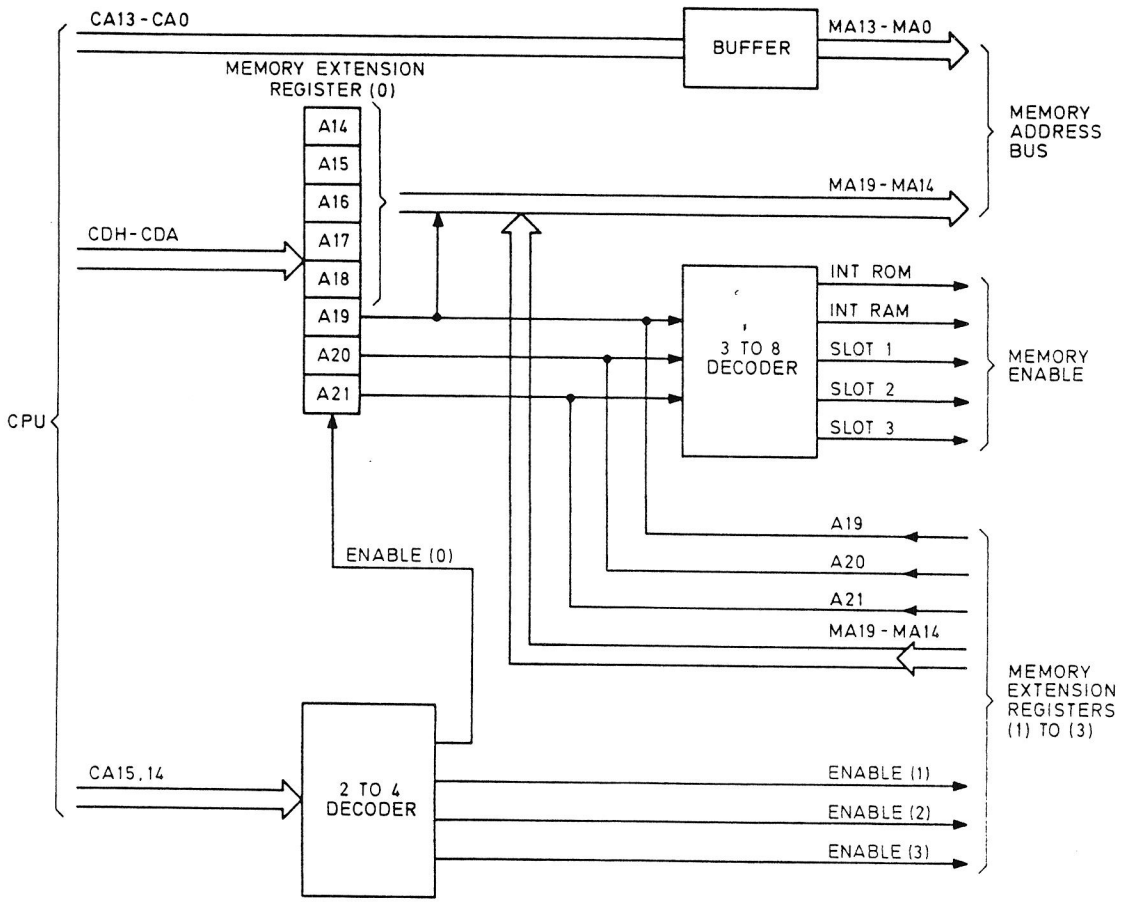


FIGURE 1.1 MEMORY ADDRESSING

6.5 Read/Write Operations (Figure 1.6)

6.5.1 Memory read/write operations are decoded by the gate array using the $\overline{M1}$, $\overline{RD}$ and $\overline{MREQ}$ inputs from the CPU, and address bits A21 - A19 held in the address extension registers.

6.5.2 **Internal EPROM (IC3).** Read cycles for IC3 are preceded by writing all 0's to bits A21 - A19 of the appropriate address extension register within IC4. When the CPU enables the register, these bits are decoded to produce the active low chip enable signal for the EPROM, output as IPCE on IC4 pin 68.

The active low output enable signal for IC3 is also decoded within IC4 from the $\overline{M1}$, $\overline{RD}$ and $\overline{MREQ}$ waveforms generated by the CPU during an instruction opcode fetch. In the appropriate combination, these signals generate ROE on IC4 pin 87, causing the EPROM to output data to IC4 on MDH - MDA from an address specified by MA15 - MA0. The latter comprises bits A13 - A0 output by the CPU as CA0 - CA13, and the bottom two bits of the gate array's address extension register. Data received from EPROM is gated within IC4 and presented to the CPU as CDH - CDA.

6.5.3 **Internal RAM (IC2).** Read/write cycles for IC2 are preceded by writing 0's into bits A21 and A20 of the appropriate address extension register and a 1 into A19. When the CPU enables the register, these bits are decoded to produce the active low chip enable signal for the RAM, output as IRCE on IC4 pin 39. The active low output enable signal for IC2 is also decoded within IC4, as in the case of the EPROM, to produce POE on IC4 pin 87. Likewise, a memory read or memory write cycle is determined by IC4 from the state of M1, MREQ and $\overline{RD}$ waveforms. IC4 pin 63 ($\overline{WR}$) is high for a read cycle and low for a write cycle.

NOTE: The printed circuit board is tracked for a 32-pin 128k byte RAM device. The circuit diagram is similarly configured. For the current 32k RAM device, pin 3 is read as pin 1, A16, A15 and POE are not used, and the $\overline{CS}$ signal (pin 28 on the 32k RAM) is VCC. In all other respects, the pinout of the two devices is identical.

6.5.4 **External RAM.** External RAM in slots 1 to 3 is accessed in a similar manner to the internal RAM except for the chip enable signals. Instead of IRCE, the gate array decodes the top two bits of the address extension register to produce individual slot enable signals SE1 to SE3 on IC4 pins 86, 93 and 91 respectively.

6.5.5 The top three bits of the address bus MA16 to MA19 are also available to each slot allowing up to 1m byte of memory to be addressed.

6.5.6 External EPROM.

TBD - Awaiting input from Cambridge Computer

6.6 Memory Refresh

6.6.1 The internal and external RAM is known as pseudo-static RAM, combining the high density/low cost benefits of a dynamic RAM with the static RAM's ability to retain data without the need for external refresh circuitry. Instead, refresh is carried out using the memory's on-chip refresh circuitry or, as is the normal case, when addressing the RAM to update the LCD display frame.

6.6.2 On-chip refresh, enabled only when the Z88 is in the coma state or the CPU is programming an EPROM, is achieved by simultaneously holding the $\overline{CE}$ line to each RAM high (ie IRCE, and SE1 to SE3), and the $\overline{OE}$/$\overline{RFSH}$ line low (ie POE). At all other times, the RAM address range produced whilst updating the LCD display frame is sufficient to keep the RAM contents refreshed.

6.6.3 The occurrence of a refresh cycle conducted by the CPU at the end of each opcode fetch instruction is sensed by the gate array from a decode of the $\overline{M1}$, $\overline{MREQ}$ and $\overline{RD}$ signals and the corresponding refresh address placed on the address bus ignored.

6.7 Bus Protection

6.7.1 As a precaution, the Z88 is forced into the coma state whenever a memory card (or peripheral card) is plugged into or removed from one of the external slots. Insertion or removal of a card is detected when the edge connector sense line is pulled down to 0V. When this occurs, the gate array generates a non-maskable interrupt to the CPU causing the latter to initiate a controlled shutdown (see also para. 11.3.3).

6.7.2 Shaping the lands on the memory card edge connectors in the region of pins 15 to 17 ensures that pin 15 (SNS) is shorted to pins 16 and 17 (0V), except when the card is fully inserted in the slot. Other edge connector lands are cut such that the sense line is grounded first before the address and data line connections are made or broken during card insertion/removal.

6.7.3 A similar scheme is adopted for the peripheral expansion card, except that the edge connector lands on the Z88 pcb are cut. In this case, two sense lines are provided in positions 1A and 24A so that the above criteria are satisfied even when the peripheral card is skewed.

7. EPROM PROGRAMMER

TBD - Awaiting input from Cambridge Computer

8. DISPLAY HANDLING

8.1 The liquid crystal display (LCD) is a sealed unit comprising a 640 x 64 dot LCD panel and the corresponding row/column drivers.

8.2 Display data is held in RAM within the Z88 and accessed by the gate array on a regular basis for output to the LCD. Power for the LCD is provided by a switched source, which is turned off when the machine is in the doze or coma state, thus blanking the display.

8.3 Data Output

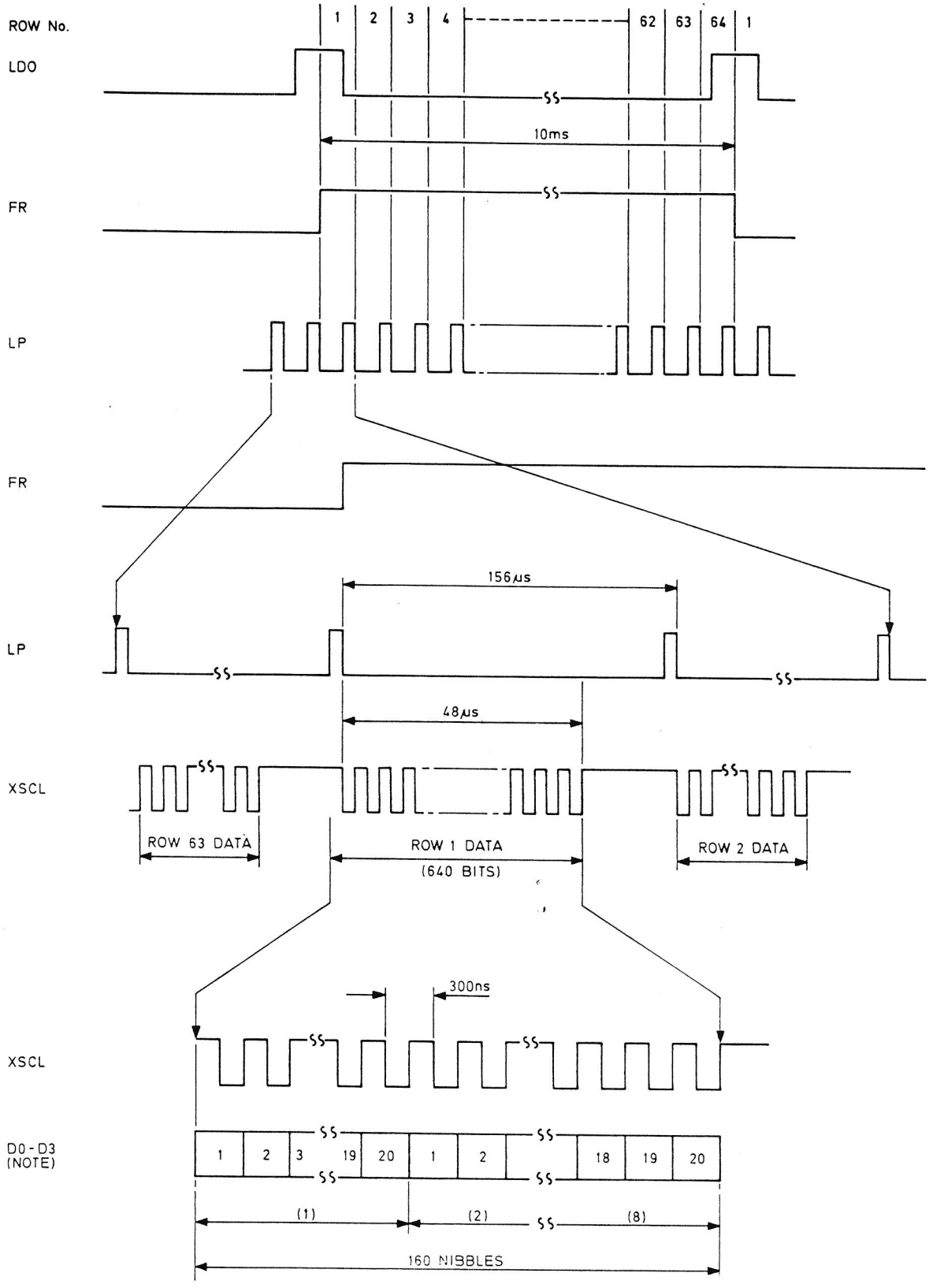
8.3.1 Referring to Figure 1.6, data is output by the gate array as nibbles of LD0 - LD3 and clocked into a 640-bit shift register within the LCD by XSCL. When data for a complete row is loaded, the array generates the line pulse LP which latches and displays the data and increments the row counter. This process is repeated 64 times, each row being displayed in quick succession giving the appearance of a complete display frame. At the end of each frame (ie once every 10 mS) the array reverses the logic state of the LCD frame signal FR. This prevents any electro-chemical reaction within the LCD degrading the display which would otherwise occur when, as in this case, the display is driven with dc. Figure 1.2 shows the timing for the gate array drive signals.

8.4 LCD Power Supply

8.4.1 DC drive for the LCD is provided by the -18V rail switched via TR8. D8 limits the voltage on TR8 collector to approximately -15.6V; RV1/RV2 and R14 control the display contrast. TR8 is turned on by TR6/7 in the presence of the 50 Hz frame pulse from the gate array on IC4 pin 46, filtered in R10/C12. When the Z88 is in the coma or doze state, the frame pulse FP is inhibited, thus turning TR6 - TR8 off and blanking the display.

9. KEYBOARD HANDLING

9.1 In any machine state other than coma, the gate array calls the keyboard scanning routines at 10 mS intervals using the non-maskable interrupt line $\overline{INT}$. (In the machine's snooze state this requires the gate array to first enable the clock to the CPU). During the routine (taking approximately 0.5 mS), the CPU systematically scans the keyboard recording which key, if any, has been pressed.



NOTE :- '(1) TO (8)' OF D0-D3 INDICATE DRIVER CHIP NUMBERS.
-IN THE DISPLAY D0 TO D3 ARE LOCATED FROM RIGHT TO LEFT.

FIGURE 1.2 LCD INTERFACE TIMING

9.2 Scanning Routine

9.2.1 The scanning method is described below with the aid of Figure 1.3. As the figure clearly illustrates, the keyboard consists of an 8 x 8 matrix, the interconnection of each row and column bridged by a normally open switch contact. The row inputs and column outputs are shown connected to separate ribbon cables SK6 and SK7, the column inputs to the CPU's high order address lines CA15 - CA8 and the row outputs to the gate array and CPU on the data bus CDH to CDA (D7 - D0).

9.2.2 When the keyboard scanning routines are entered, the CPU performs successive I/O read cycles setting the $\overline{IOREQ}$ and $\overline{RD}$ lines to the gate array low. At the same time the I/O port addresses placed on the upper half of the address bus are modified with each cycle such that address lines A15 through A8 are set low in turn, the others remaining high. (NOTE: This set of addresses is not within the I/O address range of the gate array, thus the latter will not respond to the I/O read request).

9.2.3 The sequence starts with I/O address $8F_H$ driving address line A15 low. The keyboard matrix also sees this potential on column 1 applied via D14 and the ribbon cable SK6. Thus when any of the switches on the inter-section with column 1 is pressed, the corresponding row output supplying the CPU via the second ribbon cable (SK7), is pulled low. The row outputs drive the CPU data bus and are all pulled high by RP1 when none of the keys are pressed. For example, if the 'ESC' key is pressed, row 2 drives data bus D5 (CDE) low and so on.

The sequence ends with I/O address FE_H when column 7 is addressed. In this case, operation of the '5' key drives D5 low. Clearly, the keyboard scanning routines make the distinction between the 'ESC' and '5' keys by knowing which address line is being driven.

9.2.5 Between interrupts while the machine is waiting for a keyboard input, the CPU executes a HALT instruction causing the gate array to stop the CPU clock (snooze state). In this state, address lines A15 - A8 are all low. As a result, operation of any key will cause the respective data line to be pulled low. An AND gate in the gate array, monitoring the data bus, registers the key operation and after enabling the master clock to the CPU, generates a maskable interrupt immediately requesting a keyboard scan.

9.3 Turn on Sequence

9.3.1 In the coma state, when the CPU clock is stopped, the CPU must recognise operation of both SHIFT keys in order to turn the machine on. This is achieved as described in the previous paragraph except that when in coma the CPU only holds address lines A15 and A14 low. At the same time the gate array only monitors the state of data bits D7 and D6. When both data bits are low, any two of the following keys might be pressed - right-hand SHIFT, '|—|', 'HELP' or left-hand SHIFT. To find out which, the gate arrays enables the clock to the CPU and drives the maskable interrupt line requesting an immediate keyboard scan. On detecting both SHIFT keys operated, the CPU writes to a register in the gate array prompting the latter to turn on the Z88.

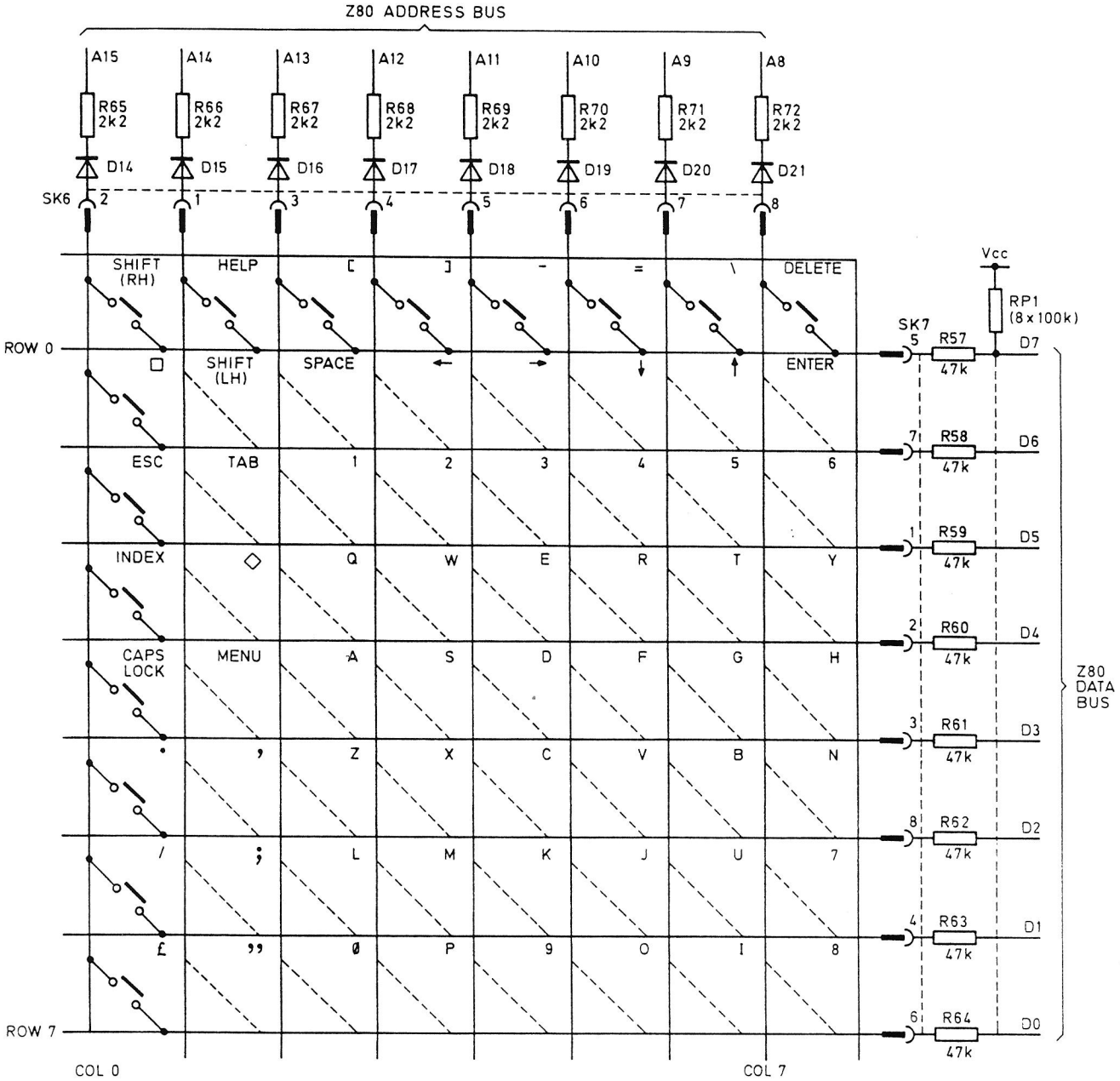


FIGURE 1.3 KEYBOARD MATRIX INTERCONNECTIONS

10. RS232C INTERFACE

10.1 The RS232C port is controlled by registers within the gate array accessed by the CPU during I/O read/write cycles to locations with address bit 4 (A3) set to 0. Single bit latches register the state of the interface control signals RTS, CTS and DCD; shift registers clocked at the selected baud rate perform the serial/parallel conversions for data transmission and reception. The physical port is presented on SK10, the conversion from RS232C levels to/from logic levels being carried out by discrete components (see Figure 1.6).

10.2 Output Circuits

10.2.1 Output circuits TXD and RTS, on the emitter of TR14 and TR15 respectively, switch between ±5V driven by outputs from the gate array on IC4 pins 37 and 38. When the gate array outputs are at +5V (logic 1) TR14 and TR15 are turned on, switching the respective output circuit to -6V. Conversely, when the array's outputs are at 0V (logic 0) TR11 and TR12 are turned on, switching the respective output circuits to +5V.

10.3 Switched Power Rails

10.3.1 It will be noted that the -6V rail for the output circuits is switched via TR16, the latter controlled by TR13/17 and the line pulse output on IC4 pin 45. Except during the coma and doze states, when the display is turned off, LP filtered by R39/C10 turns TR17, TR13 and TR16 on, enabling both the +5.5V and -6V switched power rails. In the coma and doze states, LP and the base of TR17 are both held at +5.5V turning off all three transistors and the switched power rails. In this state, with IC4 pins 37 and 38 held at +5.5V, the TXD and RTS output circuits on SK10 are allowed to float.

10.4 Input Circuits

10.4.1 Input circuits RXD, CTS and DCD are routed to IC4 pins 41, 42 and 43 via identical resistor/diode networks. Zener diodes D9 - D10 limit the excursion of the input signals to between +5.1V (logic 0) and -0.5V (logic 1); resistors R23, 26 and 29 maintain the inputs at 0V when the interface is disconnected.

10.4.2 Resistor R82 attached between the body of SK10 and the +5.5V supply available on pin 1, serves as a discharge path for any static build-up on the mating connector.

11. POWER SUPPLIES

11.1 A block diagram of the power supply circuits is given in Figure 1.5. The basis of the circuit is a flyback converter, driven by a blocking oscillator, providing voltage outputs of +12V, +5.5V, -6V and -18V. Voltage regulation is effected by sensing the +5.5V rail and turning the blocking oscillator on and off as the voltage falls or rises above this level. Input power is supplied by four AA size batteries or a plug-in mains adaptor; battery/adaptor positive is connected to ground. A 'supercapacitor' across the +5.5V rail retains its charge for a maximum of 6 minutes during battery changes, sufficient to preserve the contents of the RAM memory and keep the real-time clock running.

11.2 Input voltage and current levels are monitored together with current drawn from the +5.5V rail. Overcurrent on either supply or undervolts on the input supply causes the Z88 to adopt the coma state in which the Z80 CPU and the display are switched off to conserve battery life. Low battery voltage is a condition flagged to the CPU resulting in the 'battery low' message being displayed on the LCD display.

11.3 Battery Input Circuits

11.3.1 Referring to the circuit diagram in Figure 1.6, primary power is provided by the internal batteries or a Z88 adaptor supplying a 6.5V dc input via SK1. D23 provides reverse voltage protection; D24 isolates the battery from the negative rail when the adaptor is connected and delivering its full output.

11.3.2 TR10 monitors the input supply, generating a 'battery low' signal for the gate array on IC4 pin 96 when the battery -ve line falls below 4.2V. Provided the Z88 is not in its coma state, this signal prompts the array to send a maskable interrupt to the CPU, the CPU in turn 'writing' the 'battery low' message to the LCD. This message is not cleared until the Z88 is turned off and then on again. Under marginal battery conditions, the interrupt can be generated as the adaptor is plugged in. This occurs as a result of the battery voltage drop across D24 when the insulated shirt on the adaptor plug body initially opens the spring contact on SK1.

11.3.3 A second transistor (TR25) also monitors the input supply, driving the sense line input to the gate array on IC4 pin 94 low when the battery -ve line falls below 3.2V. At this level the battery is unable to sustain full operation of the Z88 and thus the machine must be forced into the coma state. This action is initiated by the sense signal which prompts the gate array to send a non-maskable interrupt to the CPU, the CPU in turn executing a HALT instruction. The resultant HALT signal output by the CPU to the gate array on IC4 pin 6 is responsible for triggering the shut-down sequence. Principally this entails turning off the LCD display and stopping the clock supplying the CPU.

11.3.4 A similar chain of events is triggered if the batteries are removed for replacement while the Z88 is turned on and in the snooze state. However, because in this state the clock to the CPU is stopped, the CPU will not immediately recognize the interrupt. Ordinarily this does not cause a problem, since within 10 mS of generating the interrupt the gate array restores the clock preparatory to requesting a keyboard scan. The CPU would then recognise the interrupt and take the necessary steps to shut down the machine. However, due to the limited capacity of the +5.5V storage capacitors C4/C5 and the need to conserve the charge on the supercapacitor C22 for the RAM during the battery change, shut-down must occur within approximately 1 mS of the interrupt occurring. This is effected by using the $\overline{\text{NMI}}$ to force an immediate keyboard interrupt by driving data bus D2 low via D30. The principle is described in para 9.2.5.

11.4 Power Supply and Voltage Regulator

11.4.1 The flyback converter comprises inductor L2 driven by the blocking oscillator TR5, C10 and R8. Energy stored in L2 while TR5 is turned on is released during flyback, charging the various storage capacitors via rectifiers D1 to D6.

With reference to the supply outputs, L1 and decoupling capacitors C5 and C24 to C27 together provide a smooth +5.5V supply, distributed within the Z88 as Vcc. +5.5V is chosen so as to meet the programming requirements of the plug-in EPROMs. D6 between the +5.5V and +12V rails limits the positive excursion of the +12V rail (which can rise to approximately ??V in the coma state) to +16.5V.

11.4.2 Supply regulation is provided by TR1 to TR4 which source drive for the blocking oscillator TR5. Z1 in the emitter circuit of TR1 senses the level of the +5.5V rail, turning TR1 off when the supply drops below +5.5V. TR1 off turns TR2/TR4 on sourcing drive current for TR5. As a result, TR5 is allowed to oscillate, restoring the level of the +5.5V rail. At this point, TR1 is turned on, TR1/TR4 turn off and oscillation of TR5 ceases. Feedback between TR4 emitter and TR1 base via R3 limits the gain of the regulator, preventing it from breaking into violent oscillation. R5 senses the drive current taken by TR5 turning on TR3 when the current drawn from battery exceeds ?? mA. In these circumstances, TR3 diverts drive current to TR5, shutting down the oscillator and with it the power supply.

11.4.3 TR9 monitors the current drawn from the +5.5V power rails, turning on when the emitter voltage goes sufficiently negative to forward bias the base emitter junction. This is only true when the -6V switched supply is enabled (ie the machine is not in the coma or doze state - see para. 10.3.1) and the voltage on TR1 emitter, as a result of excess current drawn from the +5.5V rail, drops to approximately 0V. Under these conditions, the voltage drop across D26 fixes TR9 emitter at approximately -0.5V and since the base is tied to 0V, TR9 turns on. TR9 turning on drives the sense line input to the gate array on IC4 pin 94, forcing the Z88 into the coma state as described in para. 11.3.3.

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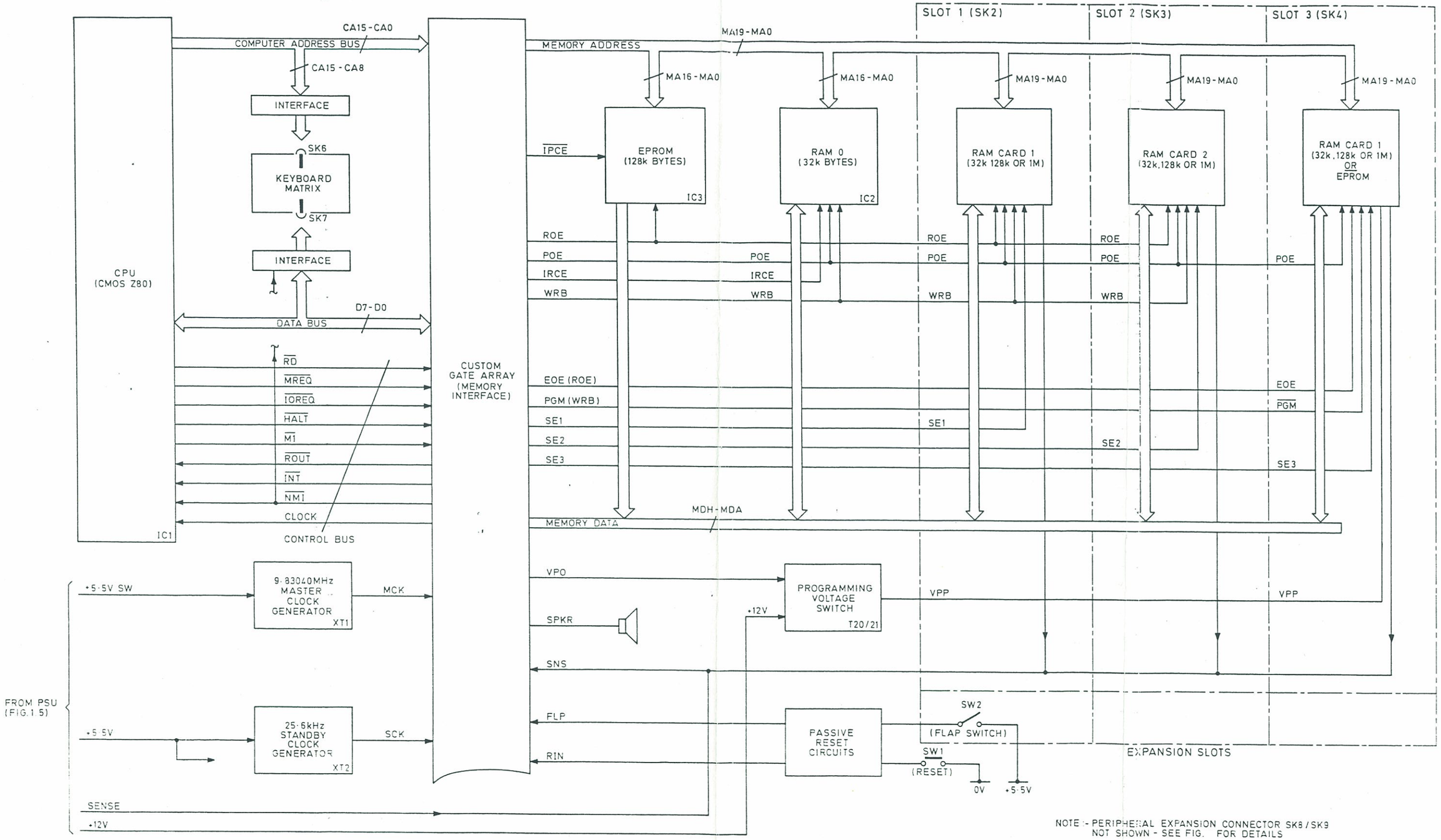

FIGURE 1.4 Z88 BLOCK DIAGRAM (PART 1)

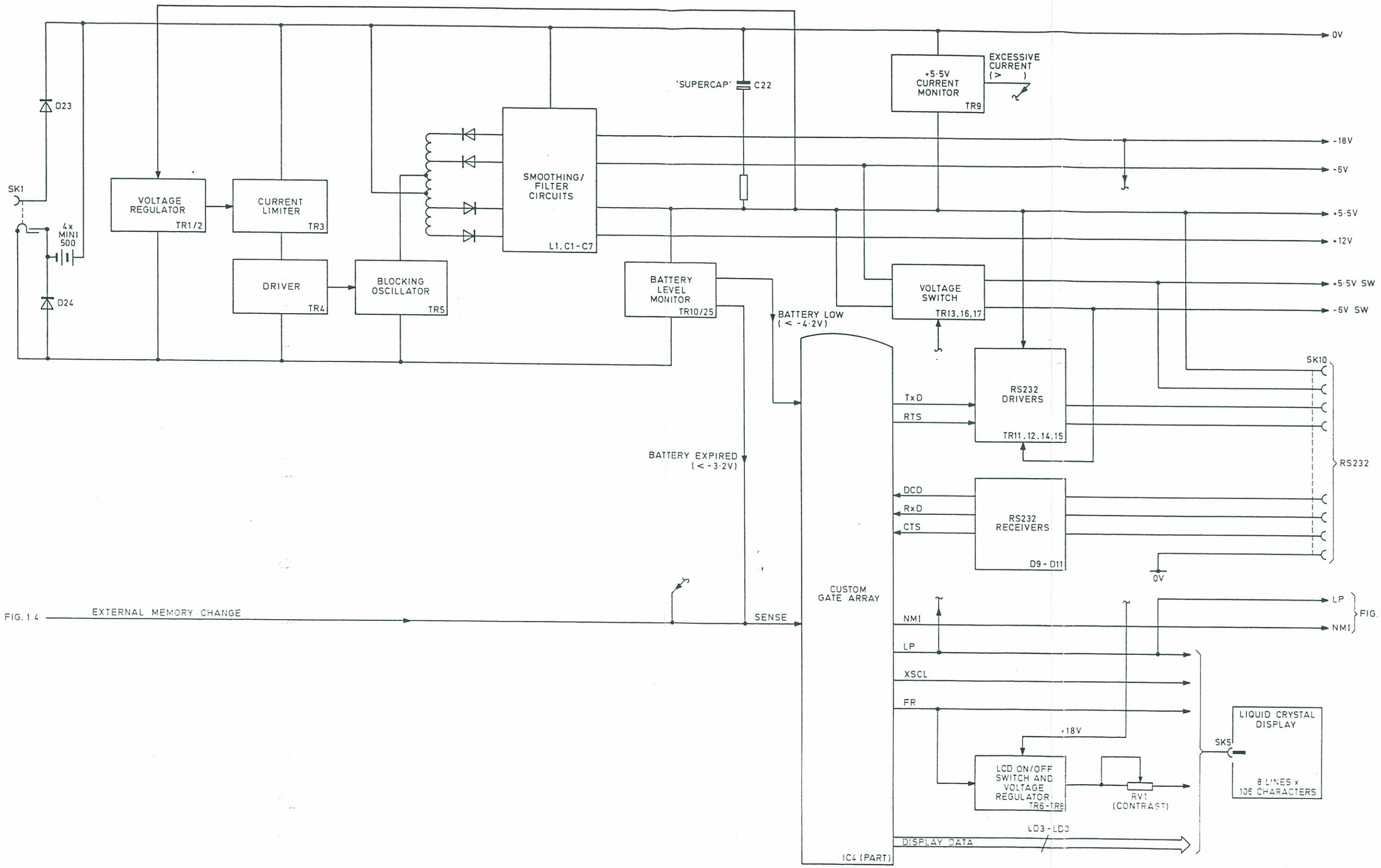

FIGURE 1.5 Z88 BLOCK DIAGRAM (PART 2)

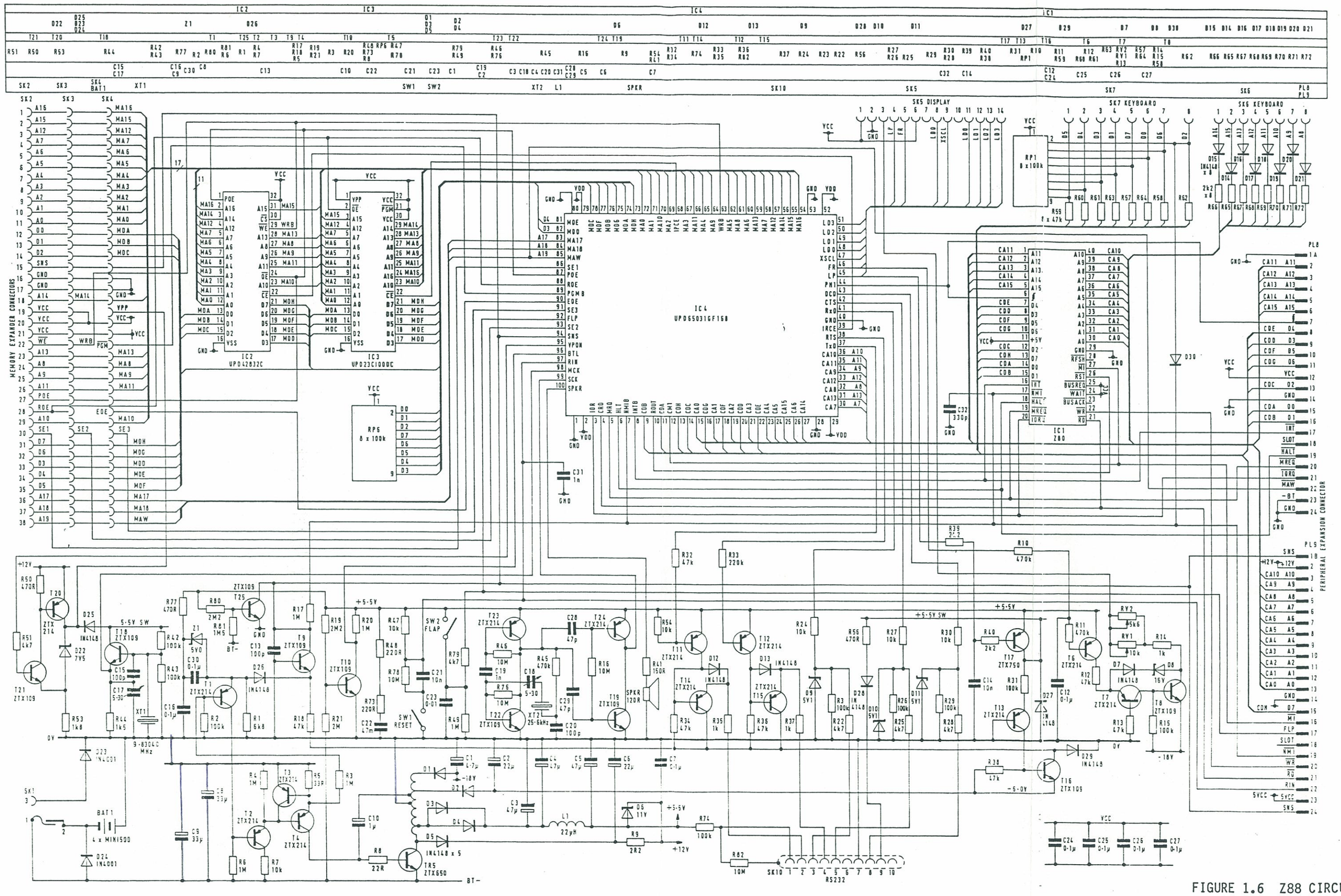

FIGURE 1.6 Z88 CIRCUIT DIAGRAM

TBD - Awaiting input from Cambridge Computer

FIGURE 1.7 MEMORY CARD
CIRCUIT DIAGRAMS