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(57) Abstract

A dynamic RAM memory device with DRAM (10) comprises a control unit (22) detecting when memory accesses are required for read, write or refresh. This unit (22) controls a voltage control circuit (26) which provides operating voltage (e.g. +5v) to the DRAM (10) but switches the voltage to a low level (e.g. 0.5v) in intervals between accesses. The low level is such that the current taken by the DRAM (10) is substantially zero.