INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(54) Title: IMPROVEMENTS IN DIGITAL COMPUTERS

(57) Abstract

A battery portable computer comprises a CPU (10), logic array (11), RAM (17) and ROM (16) and peripheral devices - keyboard (12), display (13), plug-in memory modules (18, 19, 20) and other ports (14). In order to avoid pin-limitation constraints on the logic array (11) some operations are handled without dedicated ports. The keyboard (12) has a matrix connected directly across data and address lines but so as effectively not to load these lines during normal CPU clock cycles. When the keyboard is to be serviced, the CPU clock is stopped for long enough to allow a data line (D_0-D_7) to be driven low by a walking bit on an address line (A_8-A_{15}) when the key-switch at the intersection of the lines is closed. An EPROM (20) in a specific address space range ($C0000_H$ - $FFFF_H$) can be programmed by stopping the CPU clock long enough to provide the required programming voltage to the EPROM to write a byte on the data bus (D'_0-D'_7) therein. The CPU (10) is a CMOS device which does not lose data in its internal registers when its clock is stopped.