Using the Operation Status Bits in AMD Devices

Application Note

July 2003

The following document refers to Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this document as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal documentation improvements and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

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Application Note

First generation Flash memory devices required the system CPU to execute the program and erase algorithms in software. These algorithms consisted of a complex series of operations with strict timing requirements in order to set-up, control and monitor the Flash device. Erroneous execution of these algorithms could render the Flash device inoperable thereby compromising system reliability. To eliminate concerns by system software designers AMD choose to embed the algorithms within the Flash device.

WHY ARE THE OPERATION STATUS BITS PROVIDED?

From the system point of view the Flash memory device functions both as a memory and as a peripheral to the CPU. Operation as a memory device is straight forward. Operation as a peripheral involves following a command and status protocol similar to other system peripherals. The protocol consist of JEDEC compliant command sequences which are written to the device followed by status interrogation read from the device. Through this protocol the system CPU communicates with a sophisticated state machine internal to the Flash memory device. All AMD Flash devices therefore provide Operation Status Bits to monitor the status of these embedded operations.

WHAT CAN BE DETERMINED FROM THESE STATUS BITS?

The following information can be determined by polling the Operation Status Bits:

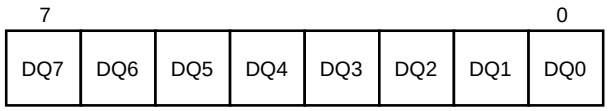
1. Program cycle completion
2. Chip Erase cycle completion
3. Sector Erase cycle completion
4. Checking if a Sector is in the Erase Suspend Mode
5. Ensuring that the Program/Erase operation has completed successfully
6. Checking if the Sector Erase time-out window is open (when issuing multiple Sector Erase commands).
7. Checking if the Write-to-Buffer Abort condition has been initiated.

WHAT ARE THE STATUS BITS PROVIDED ON AMD FLASH DEVICES?

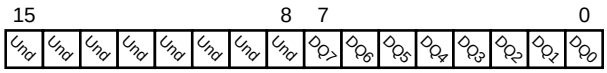
The following Operation Status Bits are provided in the status register of AMD Flash devices:

DQ7: Data# Polling
DQ6: Toggle Bit 1
DQ5: Exceeded Timing Limits Bit
DQ4: Reserved
DQ3: Sector Erase Timer Bit
DQ2: Toggle Bit 2 (not offered on all devices)
DQ1: Write-to-Buffer Abort
DQ0: Reserved

STATUS REGISTER



Status Register in 8-bit mode (BTYE# pin driven low)



Status Register in 16-bit mode (BTYE# pin driven high)

In addition to the Operation Status Bits, a Ready/Busy# (RY/BY#) pin is also provided on **most** AMD Flash devices. Checking the RY/BY# pin is another method by which the host system can determine if the Flash device has completed a Program or Erase operation. This document also discusses usage of the RY/BY# pin as an alternative to polling the Operation Status Bits wherever applicable.

HOW DO THE STATUS BITS ACTUALLY WORK?

Internally, AMD Flash devices multiplex the Data pins (DQ0-DQ7) between the memory array and the Status Register (see Figure 1). When a Program or Erase operation begins, the multiplexer switches the Data pins

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to the Status Register. The Flash device is now operating as a peripheral. By executing a read bus cycle to the Flash device the Operation Status Bits are fetched from the status register and presented on the data pins (DQ0-DQ7). After a Program or Erase operation is complete, the multiplexer switches the data pins back to the memory array. The Flash device now reverts back to operating as a memory.

Please note that Status Bits are valid after the WE# rising edge on the last command and any applicable program/erase time-outs.

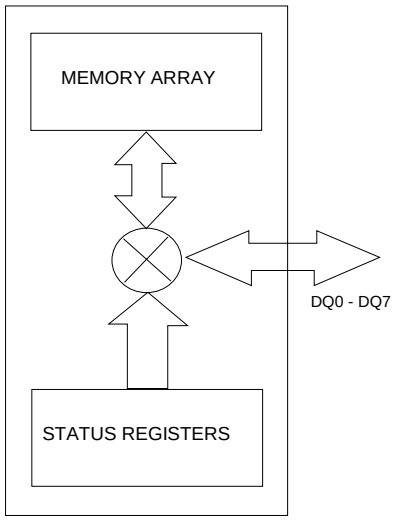


Figure 1. Data Pins Multiplexed between the Memory Array and Status Register

HOW CAN THE HOST SYSTEM ACCESS THE OPERATION STATUS BITS?

The Operation Status Bits may be accessed by a simple Read cycle. All Status Bits are valid after the rising edge of the final WE# pulse in the Program/Erase command sequence. The microprocessor may (a) continuously poll the Status Bits immediately after the Program/Erase command sequence is written or (b) periodically poll the Status Bits while performing other tasks. The designer has the option to implement the appropriate polling method depending on the specific host system. For an example see Figure 2.

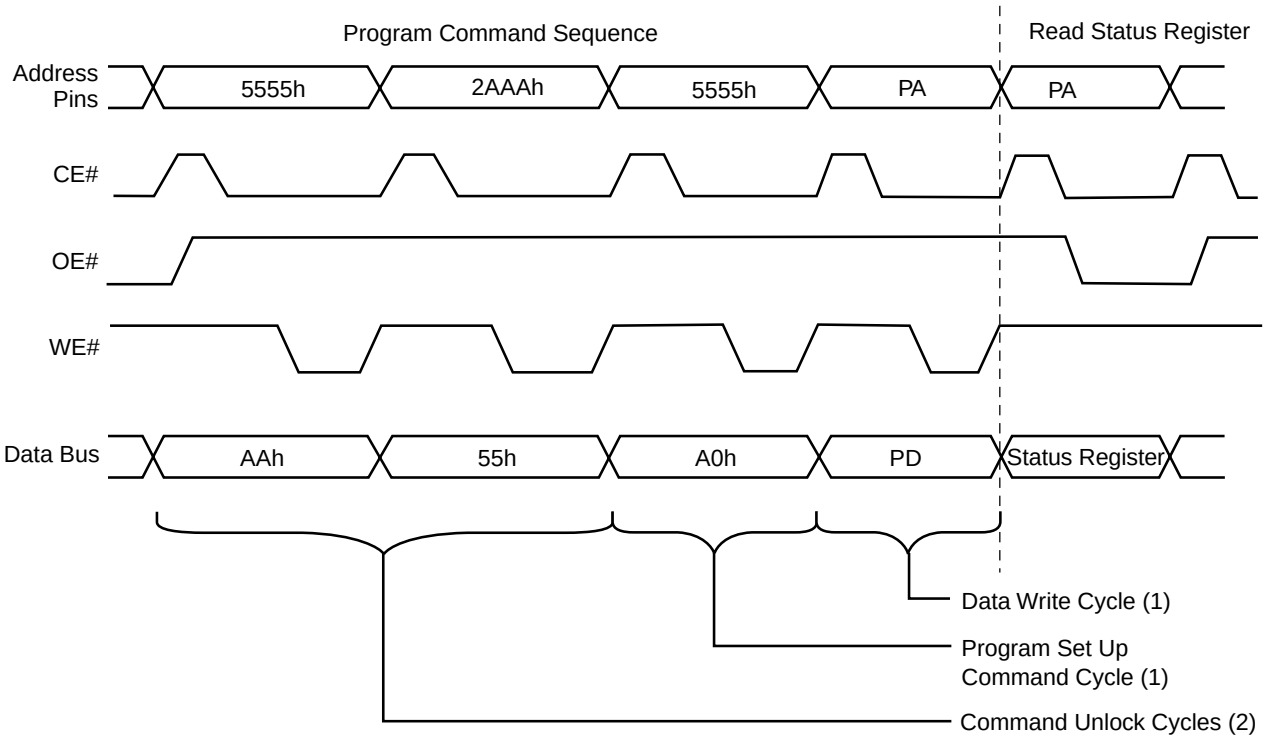


Figure 2. Example of Am29F040 Program Operation

USING THE OPERATION STATUS BITS

The Operation Status Bits provided on AMD Flash devices can be used for the following: (Using the RY/BY# pin as an alternative to the Operation Status bits is also discussed.)

1. **Checking if the device has completed a Program operation:** To determine if the Flash device has completed a Program operation the system may (a) poll DQ6 or (b) poll DQ7 or (c) check the RY/BY# pin. DQ6 and DQ7 must always be polled in conjunction with DQ5 (see Item 5, "Ensuring that the Program/Erase operation has completed successfully").

   a. Polling DQ6:

      Once the Flash device starts a Program operation, successively reading from any address will show DQ6 to be toggling i.e. if DQ6 is a "1" in the first Read cycle, it will be a "0" in the next. Once the Program operation is completed, DQ6 stops toggling and valid array data will be read in the next attempt. Refer to Figure 3 for the polling sequence.

      Note: Although DQ6 may be read from any address, AMD recommends using a consistent address throughout the polling sequence.

   OR

   b. Polling DQ7:

      Once the Flash device starts a Program operation, reading the DQ7 Status Bit yields the complement of the data last written to DQ7. Note that DQ7 must be read from the location being programmed. Once the programming is complete, DQ7 returns the true data last written to DQ7. Refer to Figure 4 for the polling sequence.

   OR

   c. Check RY/BY# pin:

      The RY/BY# pin will be "low" if the device has started the Program operation, and "high" when the operation is complete. The RY/BY# pin may be tied to the interrupt of the microprocessor. The microprocessor may then perform other tasks after issuing the program command. The RY/BY# pin will interrupt the microprocessor when the operation is complete. In the absence of a RY/BY# pin, the host system will have to rely on polling the DQ6 or DQ7 Status Bits.

2. **Checking if the device has completed an Chip Erase operation:** To determine if the Flash device has completed a Chip Erase operation the system may (a) poll DQ6, (b) poll DQ7 or (c) check the RY/BY# pin. DQ6 and DQ7 must always be polled in conjunction with DQ5 (see Item 5, "Ensuring that the Program/Erase operation has completed successfully").

   a. Polling DQ6:

      Once the Flash device starts a Chip Erase operation, successively reading from any address will show DQ6 to be toggling. Once the Chip Erase operation is completed, DQ6 stops toggling and valid array data will be read on the next attempt.

   OR

   b. Polling DQ7:

      Once the device begins a Chip Erase operation, polling DQ7 at any address returns a "0". When the Chip Erase operation is complete, DQ7 returns a "1". Refer to Figure 5 for the polling sequence.

   OR

   c. Checking RY/BY# pin:

      The RY/BY# pin will be "low" if the device has started the Chip Erase operation, and "high" when the operation is complete. The RY/BY# pin may be tied to the interrupt of the microprocessor. The microprocessor may then perform other tasks after issuing the erase command. The RY/BY# pin will interrupt the microprocessor when the operation is complete. The RY/BY# pin will then interrupt the microprocessor when the operation is completed. Note that some AMD devices do not offer the RY/BY# pin, in which case the host system will have to rely on polling the DQ6 or DQ7 Status Bits.

3. **Checking if a the device has completed a Sector Erase operation:** To determine if a particular sector has completed the Erase operation the system will have to poll (a) DQ7 or (b) DQ6 or (c) check the RY/BY# pin. DQ6 and DQ7 must always be polled in conjunction with DQ5 (see Item 5, "Ensuring that the Program/Erase operation has completed successfully").

   a. Polling DQ6:
      Once the Flash device starts a Sector Erase operation, successively reading from any address will show DQ6 to be toggling. Once the Sector Erase operation is completed, DQ6 stops toggling and valid array data will be read on the next attempt.

   OR

   b. Polling DQ7:
      Once the device starts a Sector Erase operation, reading DQ7 from an address within the sector boundary returns a "0". When the Sector Erase is complete, DQ7 returns a "1".

   OR

   c. Checking RY/BY# pin:

      The RY/BY# pin will be "low" if the device has started the Sector Erase operation, and "high" when the operation is complete. The RY/BY# pin may be tied to the interrupt of the microprocessor. The microprocessor may then perform other

tasks after issuing the erase command. The RY/BY# pin will interrupt the microprocessor when the operation is complete. Note that some AMD devices do not offer the RY/BY# pin, in which case the host system will have to rely on polling the DQ6 or DQ7 Status Bits.

4. **Checking if a Sector is in the Erase Suspend Mode:** To determine if a particular sector is in the Erase Suspend Mode the system will have to poll both the DQ2 and DQ6 Operation Status Bits together. Note: The Am29F010, Am29F100 Bulk Erase devices do not support the Erase Suspend feature.

   Polling DQ2 & DQ6:

   Once a sector is in the Erase Suspend Mode DQ2 toggles but DQ6 does not**,** with successive reads from any location within the suspended sector. Once in the Erase Suspend Mode, the device can perform a Read or Program operation in a non-erase suspended sector. When an Erase Resume command is issued the sector resumes the Erase operation and **both** DQ2 and DQ6 will continue to toggle. When the Erase operation is complete, both DQ2 and DQ6 will stop toggling. Note that some AMD devices do not offer the DQ2 Operation Status Bit, in which case this application is not feasible. Refer to Figure 6 for the appropriate polling sequence.

5. **Ensuring that the Program/Erase operation has completed successfully:** The DQ5 Status Bit indicates whether program or erase has exceeded internally specified pulse count limits. This a failure condition which signifies that the Program/Erase operation was not completed successfully. Therefore when polling for Program or Erase completion, DQ5 must also be polled in conjunction with the other Status Bits.

   Polling DQ5:

   If a Program or Erase operation is not successful the DQ5 Status Bit will be set to a “1”. Under this condition, DQ7 will not output valid data and DQ6 will continue to toggle. To acknowledge this condition and return the device to the Read mode the system must issue a Reset command. Refer to Figures 3, 4, 5 and 6 for the appropriate polling sequence.

6. **Checking if the Sector Erase time-out window is open:** All Am29xxxxx Flash devices support the erasing of multiple sectors after issuing a single Sector Erase command sequence. The sectors may be selected for Erase in any order: For example Sector 9 first and Sector 1 next, etc. A Sector Erase is a six bus cycle operation (see datasheet). There are two unlock write cycles followed by a set-up cycle. Two more unlock cycles are then followed by the actual Sector Erase command cycle (sector address + Sector Erase command: 30h). After the Sector Erase command cycle is written (6th bus cycle), the Sector Erase time-out window of 50 µs begins. The next Sector Erase command cycle must be written before this 50 µs time-out period expires. Every time the system writes an additional Sector Erase command (30h), the 50 µs time-out window is reset and another Sector Erase command cycle may be written within 50 µs. The following example illustrates the sequence to be implemented to erase 3 sectors.

6th bus cycle:	Address of the 1st sector to be erased + 30h (Sector Erase command)	50 µs time-out begins
7th bus cycle:	Address of the 2nd sector to be erased + 30h (Sector Erase command)	Time-out window is reset and 50 µs time-out begins again
8th bus cycle:	Address of the 3rd sector to be erased + 30h (Sector Erase command)	Sector Erase operation begins after 50 µs.

AMD Flash devices provide the DQ3 Status Bit to enable the system to check if the Sector Erase time-out window is open before every Sector Erase command cycle is issued.

Check DQ3:

If the Sector Erase time-out window is open, DQ3 will be a “0”. When the 50 µs time-out has expired, DQ3 will be set to a “1” which indicates that the Sector Erase operation has begun. Any attempt to write additional commands will be ignored until the ongoing Sector Erase operation is completed. To ensure that multiple Sector Erase commands have been accepted, the system software should check the status of DQ3 prior to and following each Sector Erase command cycle. Refer to Figure 7 for the polling sequence.The first check (prior to the Sector Erase cycle) is to ensure that the time-out window is still open and the second check (following the Sector Erase cycle) is to ensure that the command has been accepted. If DQ3 is a “1” on the second status check, it indicates that the 50us time-out has expired and that last sector erase command was not accepted.

7. Checking if the Write-to-Buffer Abort condition has been initiated. The DQ1 Status Bit indicates whether a Write-to-Buffer operation is in progress or has been aborted.

   Polling DQ1:

   If a Write-to-Buffer operation is in progress or has not been used, the DQ1 status Bit will be a “0”. When a Write-to-Buffer operation is aborted, DQ1 will be set to “1” to indicated the Write-to-Buffer Abort condition has been initiated.

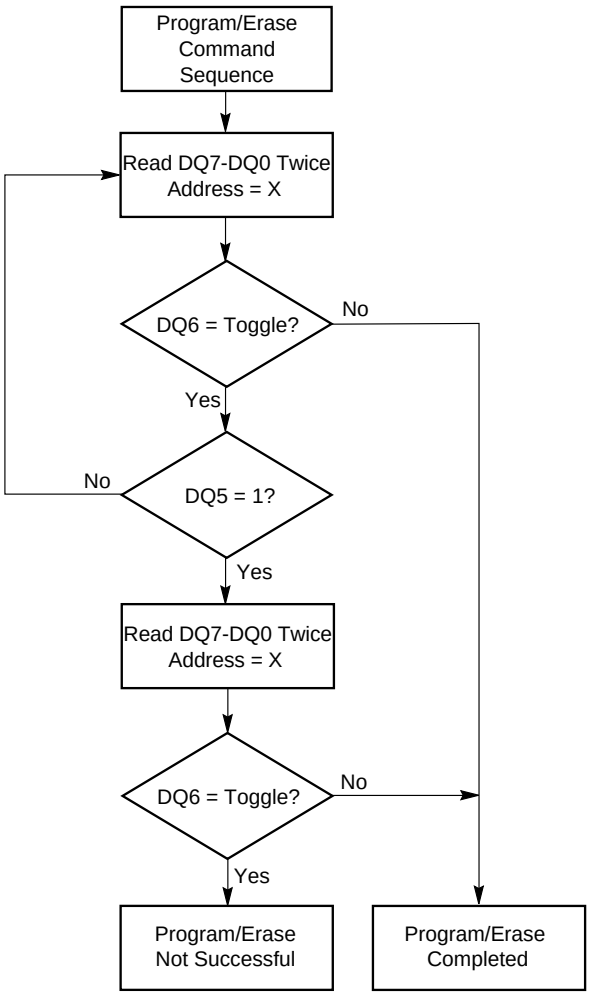
IMPLEMENTATION ISSUES

The following points must be noted when implementing the various polling algorithms discussed above:

1. To determine if DQ6 or DQ2 is toggling the CPU must:
   a. Read DQ0-DQ7
   b. Store DQ2/DQ6
   c. Read DQ0-DQ7 again
   d. Compare current DQ2/DQ6 value with that stored in step (b).
2. DQ5

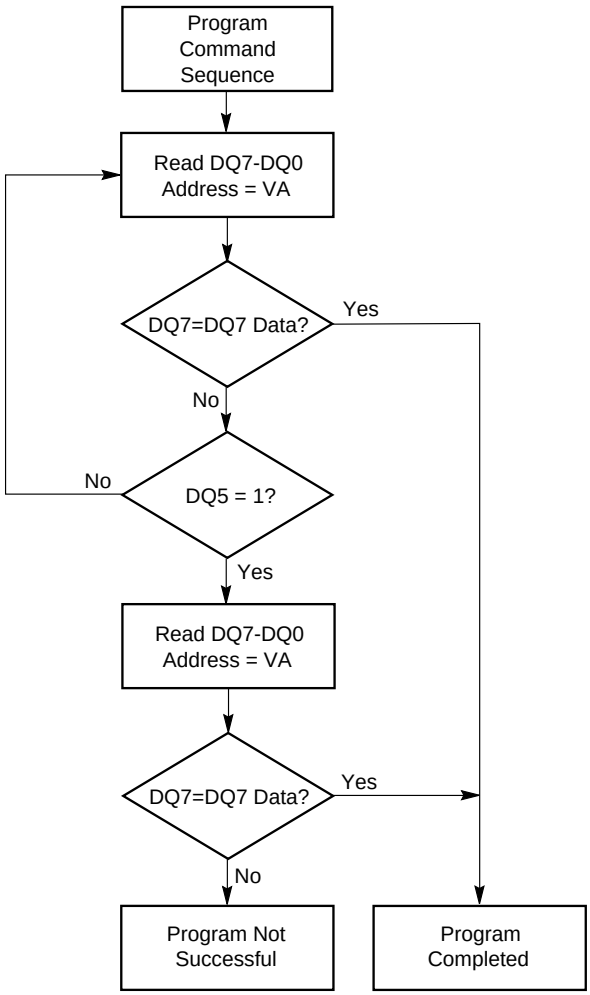
   The DQ5 Status Bit **must** be checked in conjunction with the DQ6 or DQ7 Status Bits when polling the Flash device for Program/Erase completion. See Figures 3, 4, 5 and 6.
3. The internal state machine runs asynchronously to the system CPU. The internal switching of the MUX is not synchronized with system CPU access. However, the next Read cycle will output valid data on DQ0-DQ7. Whenever the status appears to indicate that DQ5 is active, the status must be checked again to ensure that the error is valid and not a result of reading during the transition form valid status to valid data.

POLLING SEQUENCE FOR THE OPERATION STATUS BITS



Note:
PA = Program address of the location being programmed.

Figure 3. DQ6 Toggle Bit Polling Sequence for Program Completion

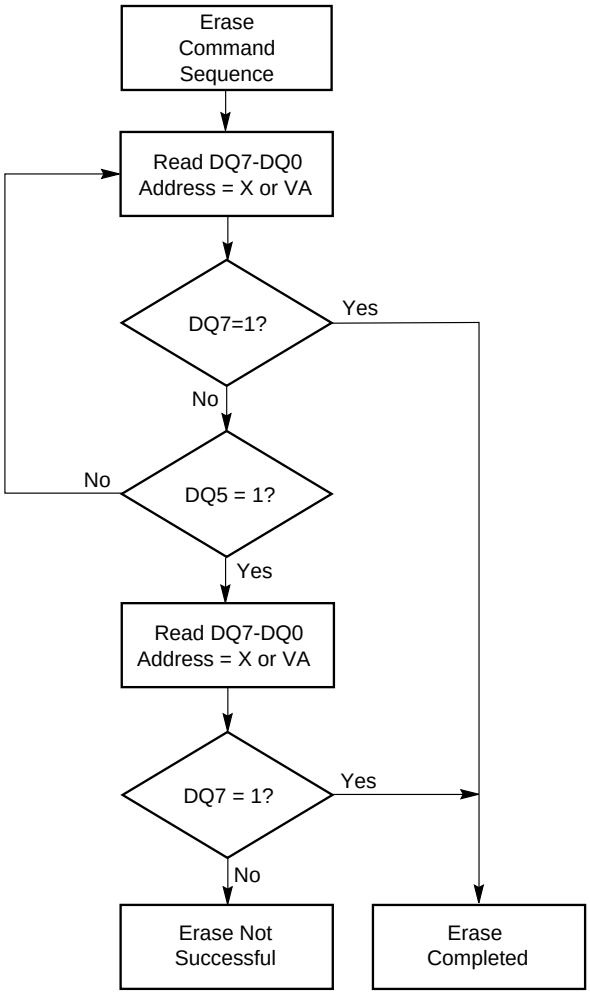


Note:
PA = Program Address of the location being programmed.

Figure 4. DQ7 Data Polling Sequence for Program Completion

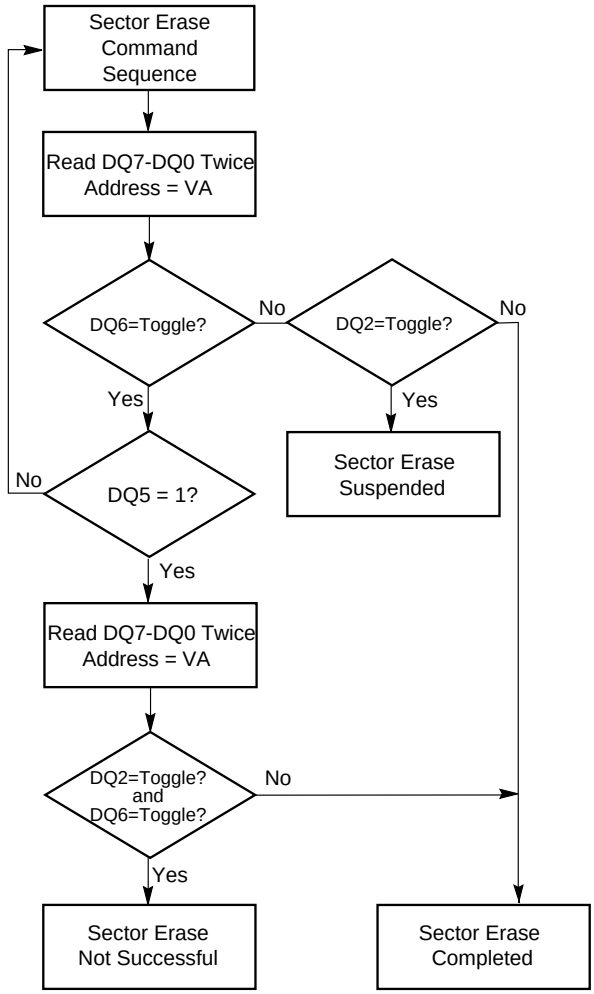
Note:

1. *The term Toggle indicates that the system will have to read the status bits consecutively and compare them to determine if they have changed states.*
2. *DQ6 toggles due to either CE# or OE#*



Note:
X = Address is a 'don't care' for Chip Erase.
VA = Address of the location being programmed.

Figure 5. DQ7 Data Polling Sequence for Erase Completion



Note:
VA = Any address within the sector.

Figure 6. DQ2 and DQ6 Polling Sequence

Note:
The term Toggle indicates that the system will have to read the status bits consecutively and compare them to determine if they have changed states.

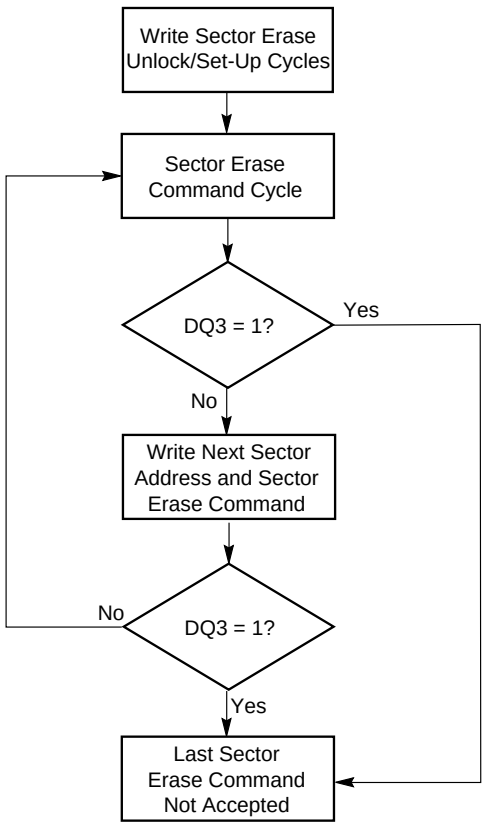


Figure 7. DQ3 Sector Erase Timer

Note:

1. *User must reset the device to return to read mode when (1) Sector Erase Timer has expired or (2) Write-to-Buffer Abort condition has occured.*

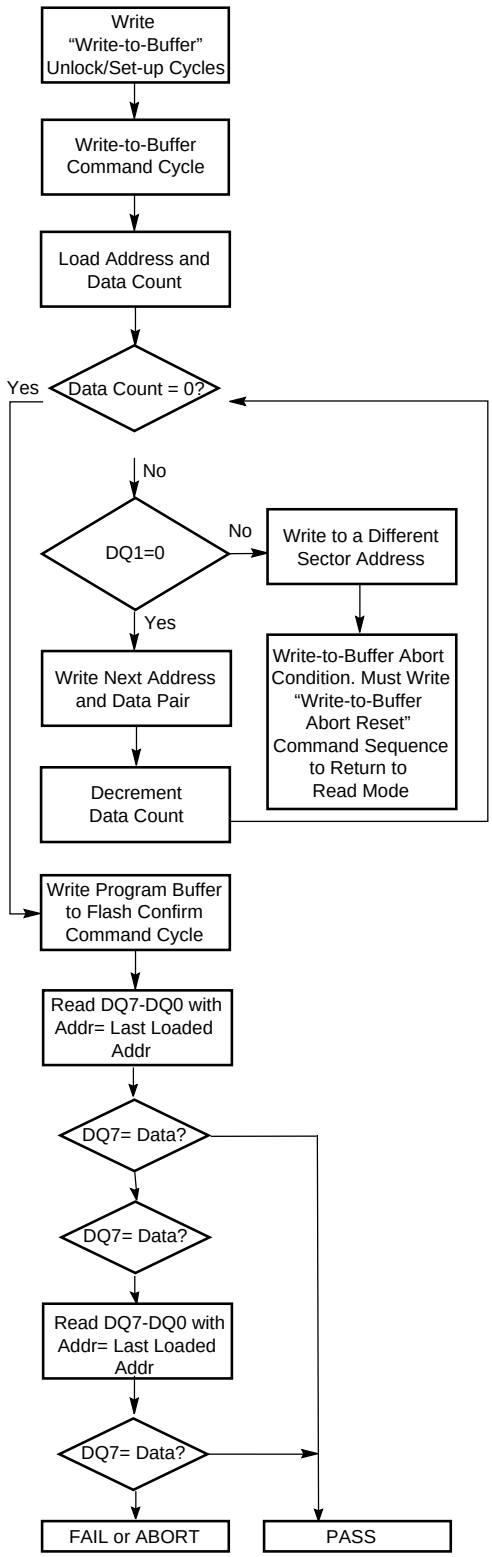


Figure 8. Write-to-Buffer Abort

SUMMARY

Applications	Option 1	Option 2	Option 3
Check if the device has completed a Program operation	Poll DQ6 Address = X Output: Toggle ⇒ Programming in progress No toggle ⇒ Programming completed	Poll DQ7 Address = Address of the location being programmed Output: Complement of DQ7 ⇒ Programming in progress True data ⇒ Programming completed	Check RY/BY# pin Address = X Output: 0 ⇒ Programming in progress 1 ⇒ Programming completed
Check if the device has completed a Chip Erase operation	Poll DQ6 Address = X Output: Toggle = Erase in progress No toggle = Erase completed	Poll DQ7 Address = X Output: 0 = Erase in progress 1 = Erase completed	Check RY/BY# Address = X Output: 0 = Erase in progress 1 = Erase completed
Check if the device has completed a Sector Erase operation	Poll DQ7 Address = Any address within the Sector Output: 0 = Erase in progress 1 = Erase completed	Poll DQ6 Address = X Output: DQ6 toggling = Erase in progress DQ6 no toggle = Erase completed	
Check if a sector is in the Erase Suspend Mode	Poll DQ2 & DQ6 Address = Any address within the Sector Output: DQ2 toggle & DQ6 no toggle = Sector erase is suspended		
Ensure that the Program/Erase operation has completed successfully	Poll DQ5 Address = X Output: 1 = Program/Erase not completed successfully		
Check if Sector Erase time-out window is open	Poll DQ3 Address = X Output: 0 = Sector Erase time-out window open 1 = Erase has begun		
Check if the Write-to-Buffer condition has been initiated	Poll DQ1 Address = Any address within the Sector Output 0 = Write-to-Buffer operation in progress 1 = Write-to-Buffer operation aborted		

Note:
X= Address don't care.

Also refer to the section on "Implementation Issues".

REVISION SUMMARY

Revision A (March 1998)

Initial release.

Revision B (August 1998)

Using the Operation Status Bits

Modified the paragraph in step 2c to indicate that the RY/BY# pin may be used to detect sector erase completion.

Revision C (February 6, 2002)

Added Write-to-Buffer Abort information to the following sections:
What can be determined from these Status Bits?
What are the Status Bits provided on AMD Flash devices?
Using the Operation Status Bits
Implementation Issues
Summary

Revision D (July 24, 2002)

Status Register

Changed Status register 8-15 to undefined.

Implementation Issues

Changed paragraph three to current state.

Figure 3. DQ6 Toggle Bit Polling Sequence for Program Completion

Figure 4. DQ7 Toggle Bit Polling Sequence for Program Completion

Modified note from VA= to PA=

Added Note 2

Figure 5. DQ7 Data Polling Sequence for Erase Completion

Figure 6. DQ2 and DQ6 Polling Sequence for Erase Completion

Modified note from VA= to SA=

Added Note 2

Figure 7. DQ3 Sector Erase Timer

Added Note

Figure 8. DQ1 Write-to-Buffer Abort

Extended diagram six more fields and added “pass.”